REMARKS

Summary of the Office Action

Claims 1-16 are pending in the application. Each of these claims stands rejected under 35 U.S.C. § 103 as being unpatentable over Park et al (U.S. Patent 6,791,558) in view of Hussain (U.S. Patent 6,801,203). The rejection of claims 1-16 is respectfully traversed.

Analysis of the Claim Rejection

Claim 1 recites, among other elements:

> a color data storage unit that in advance reads and stores color data from the frame memory at the same time when the z-data storage unit reads the z-data from the frame memory, and provides the color data to the pixel rasterization pipeline only when the result of predetermined z-test is determined to be a success in the pixel rasterization pipeline.

In rejecting claim 1 under 35 U.S.C. § 103 over the combination of Park and Hussain, the Examiner admits that Park fails to explicitly teach or suggest that the pixel cache 22 includes two separate caches and the data read from external memory into a cache at the same time. The Examiner applies Hussain as making up for these deficiencies. Specifically, the Examiner states that "Hussain teaches an efficient graphics pipeline (such as color pipeline 240 s/z pipeline 250 and texture pipeline 260 in parallel, see claim 1) with a pixel cache (three separate caches, a

color cache 245, s/z cache 255 and texture cable 265) and data pre-fetching (Fig. 3 and Abstract)." The Examiner concludes that it would have been obvious to combine the teachings of Hussain into the system of Park in order to take the best advantage of the high bandwidth of the memory system while effectively masking the latency of the memory system and delivers high throughput as taught by Hussain (Abstract and column 11, lines 3-17). Applicant submits the following in response to the Examiner's reasoning.

First, Applicant submits that the combination of references cited by the Examiner does not teach or suggest that a color data storage unit provides the color data to the pixel rasterization pipeline only when the result of predetermined z-test is determined to be a success in the pixel rasterization pipeline. Applicant notes that in the analysis of claim 1, the Office Action is silent regarding this feature. However, in the analysis of claim 2, the Examiner cites Hussain's pre-fetching FIFO 350 and column 7, lines 10-25, as teaching a color pixel buffer that reads in advance the color data from the frame memory and stores the color data in the colored data storage unit only when the result of z-test is determined to be a success in the pixel rasterization pipeline. Applicant respectfully disagrees with this analysis.

Column 7, lines 10-25, of Hussain describes a graphic pipeline 301 and pixel cache 360 that can respectively be a color pipeline and a color cache (e.g., color pipeline 240 and color cache 245 of Figure 2) or, alternatively, a stencil z-buffer pipeline and a s/z cache (e.g., s/z pipeline 250 and s/z cache 255 of Figure 2) (see column 6, lines 52-57). Figure 3 shows pre-fetch FIFO 350 coupled to pixel cache 360 which is used to store pixel data when the data is retrieved from memory sub-system 388. By queuing up the data generated by tag compare unit

310 in pre-fetch FIFO 350, memory latency is minimized by temporally separating the generation of memory requests and the actual execution of pipeline operations in graphic pipelines 301. In other words, pixel data is pre-fetched from memory sub-system 388 and stored within pixel cache 360 before it is needed *for the corresponding pipeline operation.* See column 7, lines 10-21. The pre-fetch FIFO 350, the pixel cache 360 and the graphics pipeline 301 of Figure 3 of Hussain can be independently used as a color pipeline 240 or a stencil z-buffer pipeline 250. Therefore, the description relating to Figure 3 cited by the Examiner does not teach or suggest that the FIFO 350 provides the color data to the pixel rasterization pipeline only when the result of predetermined z-test is determined to be a success in the pixel rasterization pipeline. At least because both Park and Hussain commonly fail to teach or suggest this feature of claim 1, claim 1 is believed to be patentable over these references.

Second, Applicant submits that simply because Hussain discloses parallel pipelines does not mean that this reference discloses a color data storage unit that in advance reads and stores color data from the frame memory at the same time when the z-data storage unit reads the z-data from the frame memory. As noted above, column 7, lines 18-21, teach that in the respective graphics pipelines, pixel data is pre-fetched from memory sub-system 388 and stored within pixel cache 360 *before it is needed for the corresponding pipeline operation.* This in no way teaches or suggests that the graphics pipeline 301 operating as a color pipeline 240 would read and store color data at the same time that graphics pipeline operating as s/z pipeline 250 reads the z-data from the frame memory. Simply because the pipelines may be connected in parallel

does not teach or suggest simultaneity of the data reading and storage functions of the respective pipelines.

Third, Applicant submits that Park teaches away from the combination proposed by the Examiner. More specifically, at column 7, lines 17-25, Park teaches:

> After the depth value of the present fragment image information determined as above is stored in the pixel cache memory 22 (step S106), the color value of the present fragment information is determined, and then stored in the pixel cache memory 22 to complete the pixel rasterization of the present fragment image (step S107).
>
> As described above, according to the present invention, since the depth checking of the present fragment image information is performed before the texture mapping step, the portions of the present fragment image information obscured by the previous fragment image information does not require the performing of the texture mapping, and thus the unnecessary texture mapping can be removed.

Thus, Park clearly teaches storing the depth value of the present fragment image information before the color value of the present fragment image information is stored in the

pixel cache memory 22. Park teaches that this sequential storing is advantageous in allowing that certain steps not be performed. Thus, modifying Park by the teaching of Hussain as suggested by the Examiner is contraindicated by Park.

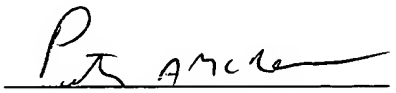
Regarding dependent claims 2-5, Applicant submits that these claims are patentable at least for the reasons that claim 1 is patentable.

Regarding independent claims 6, 11 and 14 and their respective dependent claims, the Examiner has rejected these claims for the same reason as he has rejected claims 1-5. Applicant submits that these claims are patentable at least for the same reasons that claim 1 is patentable.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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WASHINGTON OFFICE
23373
CUSTOMER NUMBER

Date: July 11, 2005